EUROPEAN COOPERATION IN SCIENCE & TECHNOLOGY

COST Action
Final Achievement Report

IC1202: Timing Analysis on Code-Level (TACLe)

(07/11/2012 to 06/11/2016)

The Action was approved by the Committee of Senior Officials (CSO) on 7-6-2012 and has the MoU reference COST 4133/12.

This report was submitted on 24-03-2017 by the Action Chair on behalf of the Management Committee in fulfilment of the requirements of the rules for COST Action Management, Monitoring and Final Assessment.

COST Association AISBL | Avenue Louise 149 | 1050 Brussels, Belgium
T +32 (0)2 533 3800 | F +32 (0)2 533 3890 | office@cost.eu | www.cost.eu

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Action leadership and participants

Leadership Positions

Position	Name	Contact details	Country of work affiliation
Chair	Prof Björn Lisper	bjorn.lisper@mdh.se +4621151709	SE

Position	Name	Contact details	Country of Nomination
Vice Chair	Prof Heiko Falk	Heiko.Falk@tuhh.de +4940428783055	DE

Working Groups

#	WG Title	# of participants	WG Leader	Country of nomination
1	Timing models for multi-cores and timing composability	35	Dr Christine ROCHANGE Christine.Rochange@irit.fr	FR
2	Tooling Aspects	25	Prof Martin Schoeberl masca@dtu.dk	DK
3	Early-stage timing analysis	15	Prof Tullio Vardanega tullio.vardanega@math.unipd.it	IT
4	Other resources than time	25	Prof Kevin Hammond kevin@kevinhammond.net	UK

Participants

COST Member Countries and Cooperating State having accepted the MoU

AT	23/10/2012	**BE**	03/02/2015	**DK**	04/07/2012	**FI**	30/07/2012	**FR**	25/07/2012
DE	05/07/2012	**EL**	09/10/2012	**HU**	08/05/2013	**IE**	26/11/2012	**IT**	25/07/2012
LT	03/10/2012	**LU**	04/05/2015	**NL**	03/09/2013	**NO**	29/11/2012	**PT**	21/08/2012
RS	21/05/2013	**ES**	18/06/2012	**SE**	12/09/2012	**UK**	19/06/2012	**MK**	05/02/2013

Other Participants

Institution Name	Country
National University of Singapore	Singapore

Summary

Main aim/ objective

The main objective of the Action is to develop industrial strength code-level timing analysis techniques for future generation embedded systems.

The Action addressed this as described below.

The Action has addressed its main objective through a number of instruments. Bi-annual joint Working Group meetings have been held, promoting the exchange of ideas both within and across the different sub-areas addressed by the Action. Activities like the work with TACLeBench, and the WCET Tool Challenge, have provided infrastucture for the comparative evaluation of timing analysis tools and techniques. The buildup of the code-level timing analysis research community has been supported by the sponsoring of the annual WCET Workshop. The supported RAC, FOPARA, HiPEAC, and EACO workshops have provided means to reach out to neighboring research communities, in areas like energy consumption, general resource analysis, and computer architecture. Other dissemination actions include invited talks at workshops in ITCs, thus spreading the knowledge of current timing analysis research to researchers from these countries, and thematic sessions at scientific meetings. Experts from timing analysis tool vendors have participated in the Action, stimulating the incorporation of research results into commercial tools. End-users of timing analysis have been involved through the Industrial Advisory Board.

The Action has put a special focus on the training and career promotion of PhD students and junior PhDs (ESRs). For this purpose, the Action has arranged two Training Schools on advanced code-level analysis techniques, a PhD student workshop, a number of focussed meetings, where ESRs have met senior experts for intense tutoring and discussions on a selected topic, and STSMs allowing ESRs to grow their network through visits to other sites in the Action. An important objective of these activities has been to form a strongly knit group of young researchers in the area of code-level timing analysis, which will form a European nucleus in this research community in the years to come.

There have been many scientific advances in the research coordinated by the Action. New and improved methods for both static (deterministic) and probabilistic timing analysis for multi-core architectures have been developed. Especially the strong advances in probabilistic methods was not foreseen, and provides a success of the project. Other advances include improved cache analysis, design principles for timing-predictable software and hardware, and WCET bound improvement by targeted symbolic execution.

In all, we believe that the Action already had a significant impact in the code-level timing analysis research area. Impact on commercial tools is foreseen within two years, and societal impact in the form of safer and less expensive time- and safety-critical embedded systems is foreseen within 2-5 years.

Action website

http://www.tacle.eu/

Achievement of MoU objectives, deliverables and additional outputs/ achievements

MoU objectives

The Action had the following specific objectives.

MoU objective	Level of achievement	Further information (hyperlink or other)
to develop improved methods for CLTA that can deliver precise timing estimates for multicore architectures	76 - 100%	Publications: Timon Kelter, "WCET Analysis and Optimization for Multi-Core Real-Time Systems", PhD thesis: http://ls12-www.cs.tu-dortmund.de/daes/media/documents/theses/kelter-phd.pdf (Part of the thesis based on collaboration with National University of Singapore, supported by STSM.) Andreas Gustavsson, Jan Gustafsson, Björn Lisper, "Timing Analysis of Parallel Software Using Abstract Execution", Proc. VMCAI'14: http://www.es.mdh.se/publications/3486-
to further develop design principles for hard-/software and systems that improve timing predictability	76 - 100%	Publications: C. B. Geyer, B. Huber, D. Prokesch, and P. Puschner, "Time-Predictable Code Execution – Instruction-Set Support for the Single-Path Approach", 15th IEEE International Symposium on Object/component/service-oriented Real-time Distributed Computing, Paderborn, Germany, June 19-21, 2013. http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=6913195&url=http%3A%2F%2Fieeexplore.ieee.org%2Fxpls%2Fabs_all.jsp%3Farnumber%3D6913195 T. Ungerer et. al. "parMERASA – Multi-Core Execution of Parallelised Hard Real-Time Applications Supporting Analysability", in the 16th Euromicro Conference on Digital System Design (DS), September 2013. http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=6628301&url=http%3A%2F%2Fieeexplore.ieee.org%2Fxpls%2Fabs_all.jsp%3Farnumber%3D6628301 First-Class Team proposal (H2020 ICT, see FP7/ H2020 Proposals and projects): cross-layer approach to make time and energy first-class citizens during SW design, by integrating these non- functional properties as types into the programming language, making compiler and OS aware of them, and by providing feasible timing and energy models (both worst- and average-case) at the hardware level.
to increase the usability of timing analysis tools through: o higher level of automation, o better integration of code-level timing analysis in development processes	76 - 100%	WCET Tool Challenge 2014 (comparative evaluation of timing analysis tools and tool chains), http://www.irit.fr/wiki/doku.php?id=wtc:start

		Publications: F. Wartel et al. "Measurement-Based Probabilistic Timing Analysis: Lessons from an Integrated-Modular Avionics Case Study", in the 8th IEEE International Symposium on Industrial Embedded Systems (SIES), June 2013. Niklas Holsti, Jan Gustafsson, Linus Källberg, Björn Lisper. Combining Bound-T and SWEET to Analyse Dynamic Control Flow in Machine-Code Programs, MRTC Research Report, Nov. 2014. http://www.es.mdh.se/publications/3841-
to promote the exchange of ideas with neighbouring research communities in order to: o enhance timing analysis by incorporating related analysis techniques, o extend timing analysis techniques to other resources than time	76 - 100%	EACO Workshop, http://www.cs.bris.ac.uk/Research/Micro/eaco-2014-w7.jsp FOPARA Workshop, http://resourceanalysis.cs.ru.nl/fopara/ Project proposals "First-Class-Team" and "TeamPlay", see "FP7/H2020 Proposals and projects" below
to enhance coordination and interaction between European researchers and tool vendors in the field of CLTA	76 - 100%	TACLeBench benchmark suite, http://www.tacle.eu/index.php/activities/taclebench Tool vendors AbsInt and Tidorum participate in the Action. Easy access to commercial tools for researchers. Example: tool aiT from AbsInt used at Training School, http://www.tacle.eu/index.php/activities/summer-schools-forums/2014-venice WCET Tool Challenge 2014 (comparative evaluation of tools), http://www.irit.fr/wiki/doku.php?id=wtc:start Publication (co-authored tool-vendor/academia): Niklas Holsti, Jan Gustafsson, Linus Källberg, Björn Lisper. Combining Bound-T and SWEET to Analyse Dynamic Control Flow in Machine- Code Programs, MRTC Research Report, Nov. 2014. http://www.es.mdh.se/publications/3841-
to influence the development of future multi-core architectures for real-time embedded systems so that CLTA requirements are considered as an integral part of the hardware design process	76 - 100%	Repeated contacts with the computer architecture research community through HiPEAC events, like: thematic session http://www.hipeac.net/thematic-session/timing-analysis-multicoremanycore-architectures HiPEAC workshop https://www.hipeac.net/events/activities/7185/tacle/ Publication: T. Ungerer et. al. "parMERASA – Multi-Core Execution of Parallelised Hard Real-Time Applications Supporting Analysability", in the 16th Euromicro Conference on Digital System Design (DS), September 2013. http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=6628301&url=http%3A%2F%2Fieeexplore.ie

		ee.org%2Fxpls%2Fabs_all.jsp%3Farnumber%3D6628301

Deliverables

The Action reported the following deliverables:

Deliverable	Timing of deliverable	Further information (hyperlink or other)

Additional outputs/ achievements

The following outputs/ achievements also resulted from the Action.

The Action reported 29 publications on the topic of the Action, co-authored by at least two Action participants from two countries participating in the Action, and for which the Action networking was necessary.

Co-authored Action publications - peer-reviewed

1. The T-CREST approach of compiler and WCET-analysis integration, Peter P. Puschner and Daniel Prokesch and Benedikt Huber and Jens Knoop and Stefan Hepp and Gernot Gebhard, 16th IEEE International Symposium on Object/Component/Service-Oriented Real-Time Distributed Computing, ISORC 2013, Paderborn, Germany, IEEE, 2013, 1-8

2. Selfish-LRU: Preemption-Aware Caching for Predictability and Performance. J. Reineke, S. Altmeyer, D. Grund, S. Hahn, C. Maiza, In Proc. RTAS 2014, IEEE, 2014

3. T-CREST: Time-Predictable Multi-Core Architecture for Embedded Systems. Martin Schoeberl, Sahar Abbaspour, Benny Äkesson, Neil Audsley, Raffaele Capasso, Jamie Garside, Kees Goossens, Sven Goossens, Scott Hansen, Reinhold Heckmann, Stefan Hepp, Benedikt Huber, Alexander Jordan, Evangelia Kasapaki, Jens Knoop, Yonghui Li, Daniel Prokesch, Wolfgang Puffitsch, Peter Puschner, André Rocha, Cláudio Silva, Jens Sparsø, and Alessandro Tocchi. Journal of Systems Architecture, Elsevier, 2015.

4. A Unified WCET Analysis Framework for Multicore Platforms. Sudipta Chattopadhyay, Lee Kee Chong, Abhik Roychoudhury, Timon Kelter, Peter Marwedel and Heiko Falk. ACM Transactions on Embedded Computing Systems (TECS) issue 13, no. 4s ACM 2014

5. Static analysis of multi-core TDMA resource arbitration delays. Timon Kelter, Heiko Falk, Peter Marwedel, Sudipta Chattopadhyay and Abhik Roychoudhury. Intl. Journal of Time-Critical Computing Systems (Real-Time Systems) issue 50, no. 2 Springer 2014 pages 185-229

6. Gabriel Fernandez, Javier Jalle, Jaume Abella, Eduardo Quinones Tullio Vardanega, Francisco Cazorla. Resource Usage Templates and Signatures for COTS Multicore Processors In Design Automation Conference (DAC) San Francisco, CA. June, 2015

7. Suzana Milutinovic, Jaume Abella, Damien Hardy, Eduardo Quiñones, Isabelle Puaut, Francisco J. Cazorla. Speeding up Static Probabilistic Timing Analysis In GI/ITG International Conference on Architecture of Computing Systems (ARCS), Porto (Portugal), March 24-27 2015

8. Jaume Abella, Damien Hardy, Isabelle Puaut, Eduardo Quiñones, Francisco Cazorla. On the Comparison of Deterministic and Probabilistic WCET Estimation Techniques. In Proc.16th Euromicro Conference on Real-Time Systems, Madrid, Spain, July 2014.

9. Contention in Multicore Hardware Shared Resources: Understanding of the State of the Art. Gabriel Fernandez, Jaume Abella, Eduardo Quinones, Christine Rochange, Tullio Vardanega, Francisco Cazorla. Workshop on Worst-Case Execution Time Analysis, Madrid, July 2014. OASICs, Dagstuhl Publishing, p. 31-40

10. Static probabilistic timing analysis for real-time systems using random replacement caches. Sebastian Altmeyer, Liliana Cucu-Grosjean, and Robert Davis. Real-Time Systems vol 51 no 1, Springer US, 2015 , pp. 77-123.

11. TACLeBench: A Benchmark Collection to Support Worst-Case Execution Time Research. H. Falk, S. Altmeyer, P. Hellinckx, B. Lisper, W. Puffitsch, C. Rochange, M. Schoeberl, R. B. Sorensen, P. Wägemann and S. Wegener. In Proceedings of the 16th International Workshop on Worst-Case Execution Time Analysis (WCET), OpenAccess Series in Informatics (OASIcs), Dagstuhl Publishing.

12. Marko van Eekelen and Kerstin Eder (Eds.). Proceedings of Resource Aware Computing (RAC2016) at ETAPS, Eindhoven. Electronic Lecture Notes in Computer Science, Volume 330, Pages 1-46 (10 December 2016)

13. PROXIMA: Improving Measurement-Based Timing Analysis through Randomisation and Probabilistic Analysis. Francisco J. Cazorla, Jaume Abella, Jan Anderson, Tullio Vardanega, Francis Vatrinet, Iain Bate, Ian Broster, Mikel Azkarate-Askasua, Franck Wartel, Liliana Cucu, Fabrice Cros, Glenn Farrall, Adriana Gogonel, Andrea Gianarro, Benoit Triquet, Carles Hernandez, Code Lo, Cristian Maxim, David Morales, Eduardo Quiñones, Enrico Mezzetti, Leonidas Kosmidis, Irune Agirre, Mikel Fernandez, Mladen Slijepcevic, Philippa Conmy, Walid Talaboulma, in Proc. 19th Euromicro Conference on Digital System Design (DSD) (special session on Mixed Criticality System Design, Implementation and Analysis), Limassol (Cyprus), August 31 - September 2 2016

14. Measurement-Based Timing Analysis of the AURIX Caches. Leonidas Kosmidis, Davide Compagnin, David Morales, Enrico Mezzetti, Eduardo Quiñones, Jaume Abella, Tullio Vardanega, and Francisco J. Cazorla, in Martin Schoeberl, ed. Proc. 16th International Workshop on Worst-Case Execution Time (WCET) Analysis, Toulouse (France), OpenAccess Series in Informatics (OASIcs) vol 5 pp. 9:1-9:10, July 5 2016

15. Mitigating Software Instrumentation Cache Effects in Measurement-Based Timing Analysis. Enrique Diaz, Jaume Abella, Enrico Mezzetti, Irune Agirre, Mikel Azkarate-Askasua, Tullio Vardanega, and Francisco J. Cazorla, in Martin Schoeberl, ed. Proc. 16th International Workshop on Worst-Case Execution Time (WCET) Analysis, Toulouse (France), OpenAccess Series in Informatics (OASIcs) vol 5 pp. 1:1-1:10, July 5 2016

16. EPC: Extended Path Coverage for Measurement-based Probabilistic Timing Analysis. Marco Ziccardi, Enrico Mezzetti, Tullio Vardanega, Jaume Abella, Francisco J. Cazorla, in Proc. 36th IEEE Real-Time Systems Symposium (RTSS), San Antonio (Texas), December 1-4 2015

17. IEC-61508 SIL 3-compliant Pseudo-Random Number Generators for Probabilistic Timing Analysis. Irune Agirre, Mikel Azkarate-Askasua, Jon Perez, Carles Hernandez, Jaume Abella, Tullio Vardanega, Francisco J. Cazorla, in Proc. 18th Euromicro Conference on Digital System Design (DSD) (special session on Mixed Criticality System Design, Implementation and Analysis), Funchal, Madeira (Portugal), August 26-28 2015

18. WCET Analysis Methods: Pitfalls and Challenges on their Trustworthiness. Jaume Abella, Carles Hernandez, Eduardo Quiñones, Francisco J. Cazorla, Philippa Ryan Conmy, Mikel Azkarate-askasua, Jon Perez, Enrico Mezzetti, and Tullio Vardanega, in Proc. 10th IEEE International Symposium on Industrial Embedded Systems (SIES), Siegen (Germany), June 8-10 2015

19. Increasing Confidence on Measurement-Based Contention Bounds for Real-Time Round-Robin Buses. Gabriel Fernandez, Javier Jalle, Jaume Abella, Eduardo Quiñones, Tullio Vardanega, and Francisco J. Cazorla, in Proc. 52nd Design Automation Conference (DAC), San Francisco

(California), June 7-11 2015

20. Seeking Time-Composable Partitions of Tasks for COTS Multicore Processors. Gabriel Fernandez, Jaume Abella, Eduardo Quiñones, Luca Fossati, Marco Zulianello, Tullio Vardanega, and Francisco J. Cazorla, in Proc. 18th IEEE Symposium On Real-Time Computing (ISORC), Auckland (New Zealand), April 13-17 2015

21. Introduction to Partial Time Composability for COTS Multicores. Gabriel Fernandez, Jaume Abella, Eduardo Quiñones, Luca Fossati, Marco Zulianello, Tullio Vardanega, and Francisco J. Cazorla, in Proc. 30th ACM/SIGAPP Symposium On Applied Computing (SAC), Salamanca (Spain), April 13-17 2015

22. Timing Analysis of an Avionics Case Study on Complex Hardware/Software Platforms. Franck Wartel, Leonidas Kosmidis, Adriana Gogonel, Andrea Baldovin, Zoe Stephenson, Benoit Triquet, Eduardo Quinones, Code Lo, Enrico Mezzetti, Ian Broster, Jaume Abella, Liliana Cucu-Grosjean, Tullio Vardanega, and Francisco Cazorla, in Proc. 18th Design, Automation and Test in Europe Conference (DATE), Grenoble (France), March 9-13 2015

23. Computing Safe Contention Bounds for Multicore Resources with Round-Robin and FIFO Arbitration. Gabriel Fernandez, Javier Jalle, Jaume Abella, Eduardo Quiñones, Tullio Vardanega, Francisco J. Cazorla, in IEEE Transactions on Computers, to appear

24. Fitting Processor Architectures for Measurement-Based Probabilistic Timing Analysis. Leonidas Kosmidis, Eduardo Quiñones, Jaume Abella, Tullio Vardanega, Carles Hernandez, Andrea Gianarro, Ian Broster, and Francisco J. Cazorla. Elsevier Journal of Microprocessors and Microsystems, Volume 47, Part B, Pages 287–302, November 2016

25. Parallelizing Industrial Hard Real-time Applications for the parMERASA Multi-core. Theo Ungerer, Christian Bradatsch, Martin Frieb, Florian Kluge, Jorg Mische, Alexander Stegmeier, Ralf Jahr, Mike Gerdes, Pavel Zaykov, Lucie Matusova, Zai Jian Jia Li, Zlatko Petrov, Bert Boddeker, Sebastian Kehr, Hans Regler, Andreas Hugl, Christine Rochange, Haluk Ozaktas, Hugues Casse, Armelle Bonenfant, Pascal Sainrat, Nick Lay, David George, Ian Broster, Eduardo Quiñones, Milos Panic, Jaume Abella, Carles Hernandez, Francisco J. Cazorla, Sascha Uhrig, Mathias Rohde, and Arthur Pyka, ACM Transactions on Embedded Computing Systems, Volume 15 Issue 3, Article No. 53, July 2016

26. Randomized Caches Can Be Pretty Useful to Hard Real-Time Systems. Enrico Mezzetti, Marco Ziccardi, Tullio Vardanega, Jaume Abella, Eduardo Quiñones, and Francisco J. Cazorla, Leibniz Transactions on Embedded Systems Volume 2, issue 1, 2015

27. Niklas Holst,Jan Gustafsson. Linus Källberg, and Björn Lisper. Analysing Switch-Case Code with Abstract Execution. In Francisco J. Cazorla, ed. Proc. 15th International Workshop on Worst-Case Execution Time Analysis (WCET 2015), OpenAccess Series in Informatics (OASIcs), Dagstuhl Publishing, vol 47, pp. 85-94, July 2015,

28. Stefan Bygde, Björn Lisper, and Niklas Holsti. Improved Precision in Polyhedral Analysis with Wrapping. In Science of Computer Programming vol. 133 pp 74-87, 2016

29. Sebastian Altmeyer, Björn Lisper, Claire Maiza, Jan Reineke, and Christine Rochange. D{WCET and Mixed-Criticality: What does Confidence in {WCET} Estimations Depend Upon? In Francisco J. Cazorla, ed. Proc. 15th International Workshop on Worst-Case Execution Time Analysis (WCET 2015), OpenAccess Series in Informatics (OASIcs), Dagstuhl Publishing, vol 47 pp. 65-74, 2015.

Projects

The Action reported 12 project(s) and 4 proposal(s) resulting from the Action networking.

Key details of the projects are shown below

1. ARGO
   (H2020)
2. Time-predictable Control Systems (PREDICT)
   (National)
3. Multi-dimensional quality control for e-business applications
   (Trans-national - Bi-lateral project between Serbia and Slovenia)
4. RePhrase: Refactoring Parallel Heterogeneous Resource-Aware Applications
   (H2020)
5. ParaFormance: Democratising Parallel Software Development
   (National)
6. Discovery: Pattern Discovery and Program Shaping for Manycore Systems
   (National)
7. CONIRAS -- Kontinuierliche nicht-intrusive Laufzeitanalyse von SoCs
   (National)
8. ASSUME -- Affordable Safe & Secure Mobility Evolution
   (National)
9. ARAMiS II -- Entwicklungsprozesse, Methoden, Werkzeuge und Plattformen für sicherheitskritische Multicore Systeme
   (National)
10. EMPHASE -- Integrierte energiesparende Multi-Prozessorplattform für autonomes elektrisches Fahren
    (National)
11. P-SOCRATES (Parallel Software Framework for Time-Critical Many-core Systems)
    (FP7)
12. CAPACITES: embedded hard real-time software on a many-core platform
    (National)

Other outputs / achievements

The following other outputs/ achievements contributing to the COST mission resulted from the Action:

1. Unforeseen progress as regards probabilistic code-level timing analysis. Collaborations supported by the Action has led to several co-authored papers (see "Action publications). Probabilistic analysis was not targeted in the objectives in the MoU, but has shown to be a promising technique in particular for timing analysis for multi-core architectures.

2. WCET Workshop:

   The annual WCET Workshop has grown to attract 40+ participants, and it is now the biggest satellite workshop of the ECRTS conference. TACLe has supported the workshop, and financed the open access proceedings:

   WCET Workshop 2013 (http://wcet2013.imag.fr/), open access proceedings:
   http://drops.dagstuhl.de/opus/portals/oasics/index.php?semnr=13007

   WCET Workshop 2014 (http://www.uni-ulm.de/en/in/wcet2014.html), open access proceedings:
   http://drops.dagstuhl.de/opus/portals/oasics/index.php?semnr=14005

   WCET Workshop 2015
   (https://www.bsc.es/news/events/15th-international-workshop-worst-case-execution-time-analysis-wcet-2015-lund-sweden-7th-july), open access proceedings:
   http://drops.dagstuhl.de/portals/oasics/index.php?semnr=15010

   WCET Workshop 2016 (https://wcet2016.compute.dtu.dk/), open access proceedings:
   http://drops.dagstuhl.de/opus/portals/oasics/index.php?semnr=16025

3. RAC workshop (http://resourceanalysis.cs.ru.nl/rac2016/): a workshop on resource-aware computing where TACLe financed the open access proceedings: http://www.sciencedirect.com/science/journal/15710661

Impacts

The Action reported the following impact(s):

Description of the impact, i.e. what will change, and for whom, as a result of what the Action achieved	Type of impact	Timing of impact
Improved timing analysis methods for multi-core architectures	• Scientific / Technological	Achieved
Design principles for timing-predictable HW/SW systems	• Scientific / Technological	Achieved
Improved methods for general resource analysis, including time and energy consumption	• Scientific / Technological	Achieved
Improved commercial tools for timing analysis	• Economic	Foreseen within 2 years
Safer and less expensive time-critical systems due to better tools, and methods, for timing analysis, and timing-predictable parallel hardware	• Societal	Foreseen 2-5 years

Dissemination and exploitation of Action results

Dissemination and exploitation approach of the Action

The Action's dissemination and exploitation approach as well as all activities undertaken to ensure dissemination and exploitation of Action results and the outcomes of these activities are described below.

The Action's dissemination approach has been to reach out to the research community through channels such as online, open access proceedings from workshops, and thematic sessions at meetings. The dissemination activities are listed under "Dissemination Meetings", and "Other Dissemination Activities". The Action did not have any dissemination activities to reach an audience outside the scientific community. The Action did not have any specific exploitation activities. The approach has rather been to integrate technical experts from timing analysis tool vendors as regular members of the Action, taking part in the activities of the Action. Commercial tools have also been used at the Training Schools organised by the Action. The Action had an Industrial Advisory Board (IAB), with experts from timing analysis end-users mainly within automotive and avionics. The main purpose with the IAB was to provide end-user feedback on the techniques and tools developed within the Action. While not being a direct exploitation activity, the IAB has helped paving the way for future exploitation by pointing out industrially relevant research directions.

Dissemination meetings funded by the Action

The Action funded Dissemination Meetings as shown below.

Title	SQAMIA Workshop		
Date	19-09-2014 to 22-09-2014	**Country**	Croatia
Event	SQAMIA Workshop 2014		

Title	SQAMIA Workshop		
Date	29-08-2016 to 31-08-2016	**Country**	Hungary
Event	SQAMIA Workshop 2016		

Other dissemination activities

The Action also undertook the following dissemination activities.

Activity	RAC Workshop proceedings
Target	Researchers in resource-aware computing and related areas
Outcome	Documentation of the workshop presentations in the form of online, open access proceedings
Link	http://www.sciencedirect.com/science/journal/15710661

Activity	WCET Workshop 2013 proceedings
Target	Researchers in code-level timing analysis and related areas
Outcome	Documentation of the workshop presentations in the form of online, open access proceedings
Link	http://drops.dagstuhl.de/opus/portals/oasics/index.php?semnr=13007

Activity	WCET Workshop 2014 proceedings
Target	Researchers in code-level timing analysis and related areas

Outcome	Documentation of the workshop presentations in the form of online, open access proceedings
Link	http://drops.dagstuhl.de/opus/portals/oasics/index.php?semnr=14005

Activity	WCET Workshop 2015 proceedings
Target	Researchers in code-level timing analysis and related areas
Outcome	Documentation of the workshop presentations in the form of online, open access proceedings
Link	http://drops.dagstuhl.de/portals/oasics/index.php?semnr=15010

Activity	WCET Workshop 2016 proceedings
Target	Researchers in code-level timing analysis and related areas
Outcome	Documentation of the workshop presentations in the form of online, open access proceedings
Link	http://drops.dagstuhl.de/opus/portals/oasics/index.php?semnr=16025

Activity	Thematic session on timing analysis at HiPEAC Fall Meeting 2013
Target	Researchers in computer architecture
Outcome	Several researchers in computer architecture joined the Action
Link	http://www.hipeac.net/thematic-session/timing-analysis-multicoremanycore-architectures

Exploitation activities

The Action undertook the following activities to ensure exploitation (use, in particular in a commercial context) of the Action's achievements.

No input provided by the Action

Action Success(es)

The Action's two most significant successes were the following

- There has been considerable progress regarding probabilistic code-level timing analysis within the research coordinated by the Action, and several coauthored papers by members of the Action have appeared. Probabilistic analysis provides a way to handle timing analysis for software running on parallel architectures such as multi-core processors, where it can be very hard to find both tight and completely safe upper bounds on execution time. The probabilistic methods provide an alternative for applications where some timing violations can be accepted as long as their probability is low enough. In reality this is a common scenario also in many safety-critical applications. Probabilistic analysis was not targeted in the objectives in the MoU, and the progress in this area was unforeseen.
- The TACLe-supported annual WCET Workshop, which is a satellite workshop to the ECRTS conference (a major international conference in the real-time area), has become a big success. It has grown to attract 40+ participants, it is now the biggest satellite workshop of the ECRTS conference, and it has become the main event in the code-level timing analysis area. Each submission is reviewed by at least three reviewers, which ensures the high quality of the accepted papers. The proceedings are published online, with open access. The WCET workshop is now firmly established, and will continue to be a recurring event also after the end of the Action.

Action Expenditure

The table below shows the budget allocated to the Action for each Grant Period.

#	Grant Period	Start Date	End Date	Budget allocated to Action (EUR)
1	IC1202-20130212	1-3-2013	31-7-2014	165,600.00 (EUR)
2	CGA-IC1202-2	1-8-2014	31-7-2015	123,763.00 (EUR)
3	CGA-IC1202-3	1-8-2015	30-4-2016	78,234.50 (EUR)
4	AGA-IC1202-4	1-5-2016	6-11-2016	58,063.50 (EUR)